# IMAPS NE 45

## A HETEROGENEOUS SIP SOLUTION FOR RF APPLICATIONS

May 1st 2018

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I3 MICROSYSTEMS INC PROPRIETARY INFORMATION

# A HETEROGENEOUS SIP SOLUTION FOR RF APPLICATIONS

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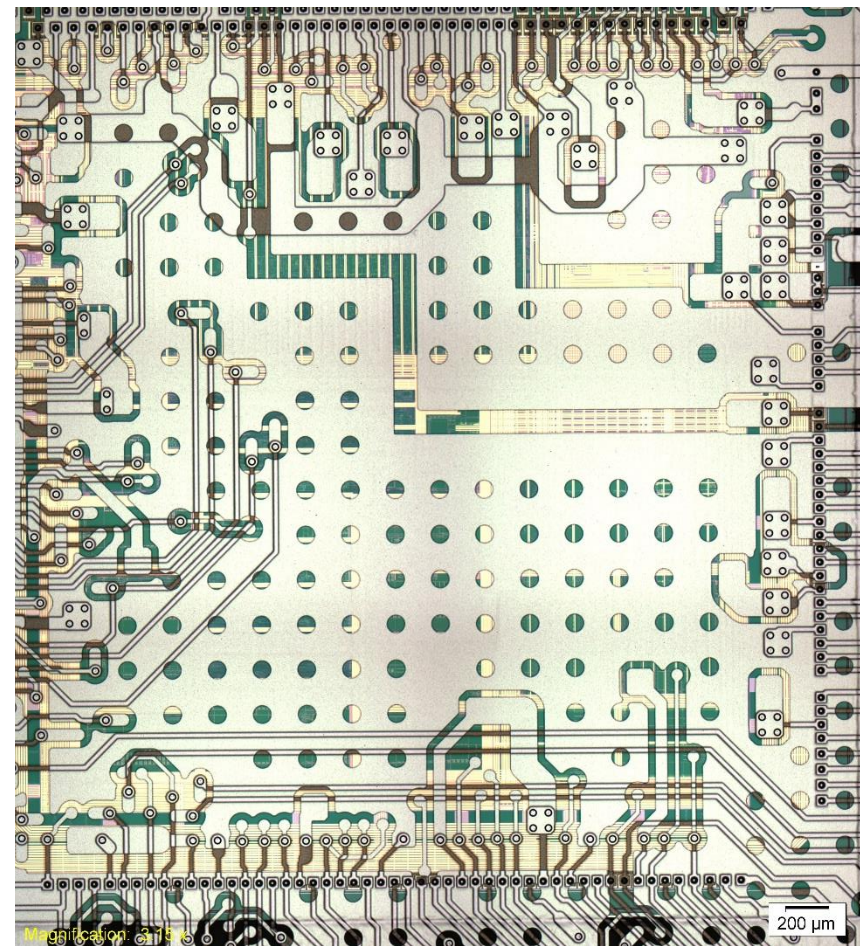
BAE SYSTEMS
INSPIRED WORK

- Presentation Content
  - DARPA ACT TA2 Project Brief
  - i3 Microsystems Overview
  - i3 Electronics Overview
  - HSIP Fabrication
  - HSIP Fabrication Results
  - Conclusion




*Typical Routing Layer in HSIP Technology*

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# DARPA ACT Project Overview

BAE SYSTEMS
INSPIRED WORK

- DARPA ACT TA2 Program (Arrays at Commercial Timescales)
  - System architecture for scalable and reconfigurable phased array that is achieved through vertical integration of devices
- Georgia Tech Research Institute
  - Prime Contractor
- BAE Systems – subcontractor to GTRI
  - Ben McMahon
- Aurora Semiconductor LLC, operations purchased by **i3 Microsystems Inc.**
  - Subcontractor to BAE

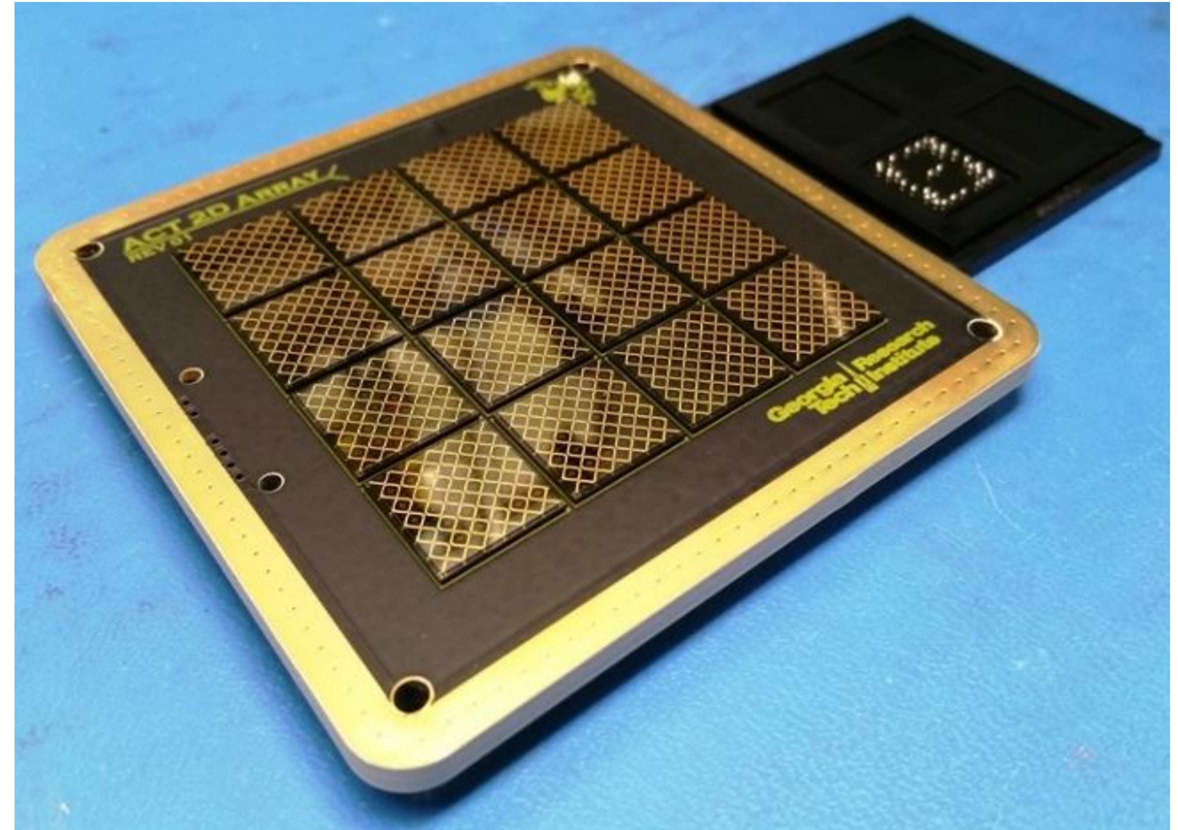


*Image courtesy of Georgia Tech Research Institute, 2017*

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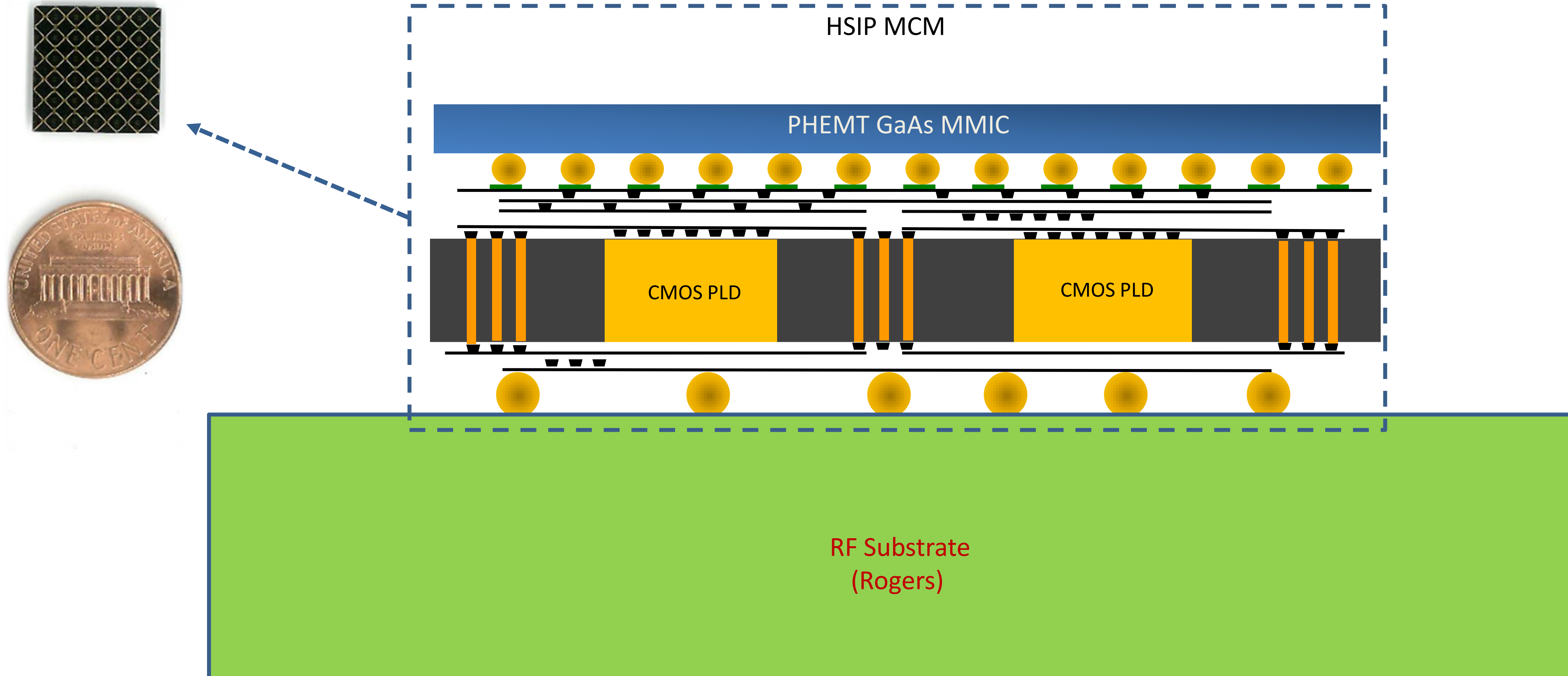
# DARPA ACT Project Overview

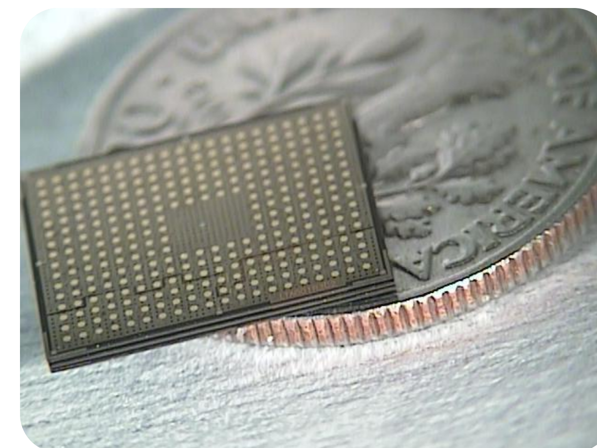



*Images courtesy of BAE Systems, 2018*

# i3 Microsystems Overview



- Organizational History
- HSIP Benefits
- Die Harvesting – Die Extraction & Recovery (DER) Services
- HSIP Reliability Baseline



*Stacked HSIP Module*
*24 Total Metal Layers*
*Double-Sided BGA Interface*

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# i3 Microsystems Overview

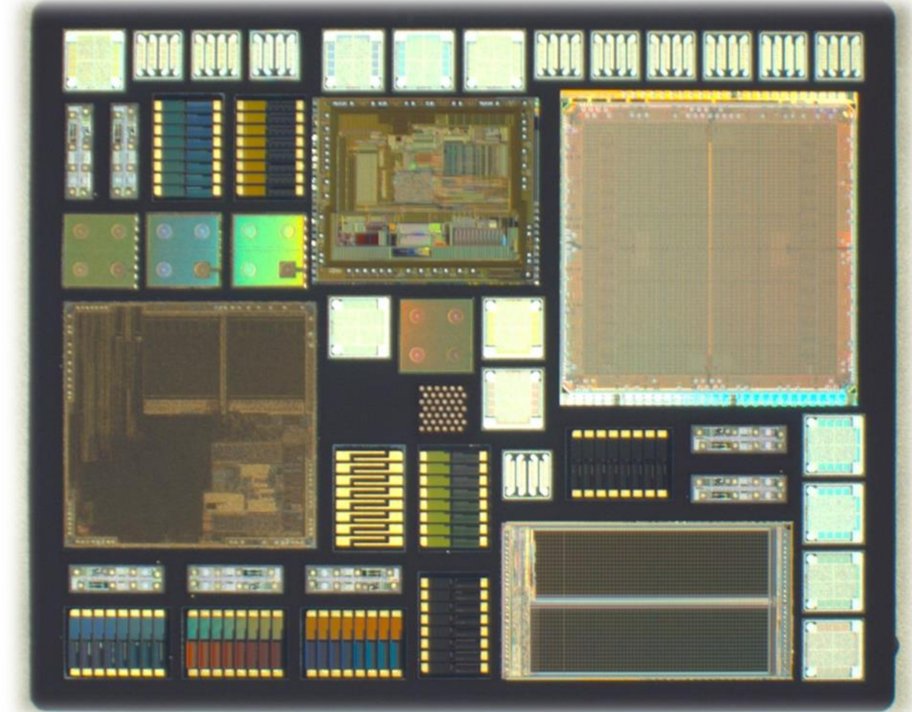
BAE SYSTEMS
INSPIRED WORK

- Organizational History
  - Operation purchased by i3 Electronics in January 2018
  - Formerly operated as Aurora Semiconductor LLC as of 2016
  - Facility established by Draper Laboratory in 2009
  - Trusted Foundry and ITAR Certified
  - ISO-9000:2008 compliant, cert 2015 in Q3

*Our Class-100 Cleanrooms are located in Saint Petersburg, Florida*

# i3 Microsystems Overview

- Organizational History
  - Our HSIP is an embedded-IC interposer solution for high-reliability product spaces
  - Our technology was clandestinely developed for government programs but is available in the USA now as a commercial foundry service



*Typical highly-integrated digital HSIP module containing heterogeneous components*

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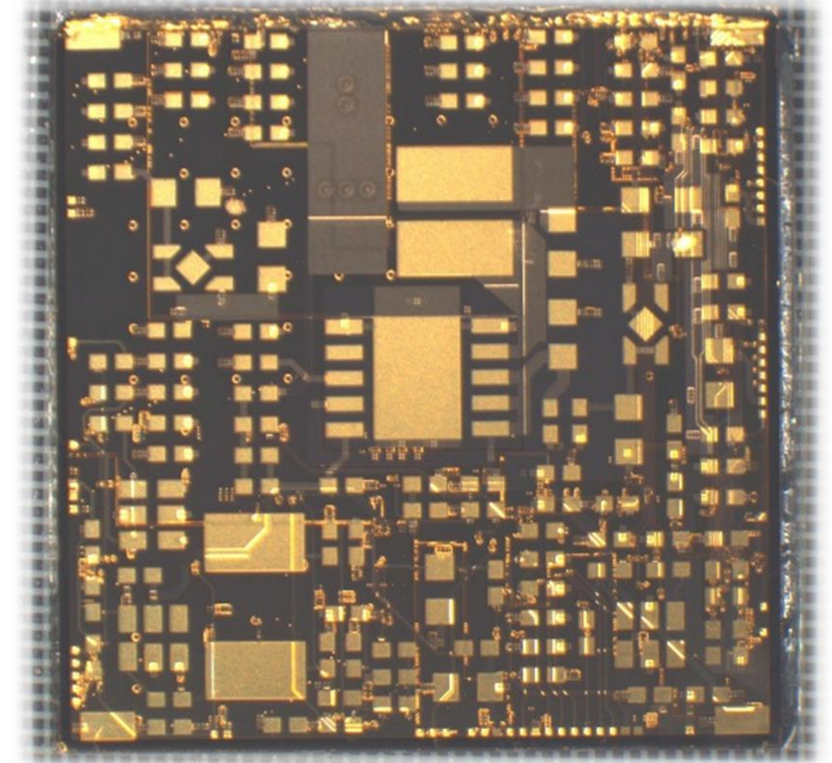
# i3 Microsystems Overview

BAE SYSTEMS
INSPIRED WORK

- HSIP Benefits
  - Potential to connect all device technologies – MEMs, sensors, memory, analog, controllers etc.; and all source substrates: Si, GaAs, InP, glass devices – into one package
  - Uses TMV (Thru Mold Via) with no wire bonds or separate interposers
  - Up to 7 interconnect metal layers per side



*Completed HSIP Module ready for assembly of additional SMT components*

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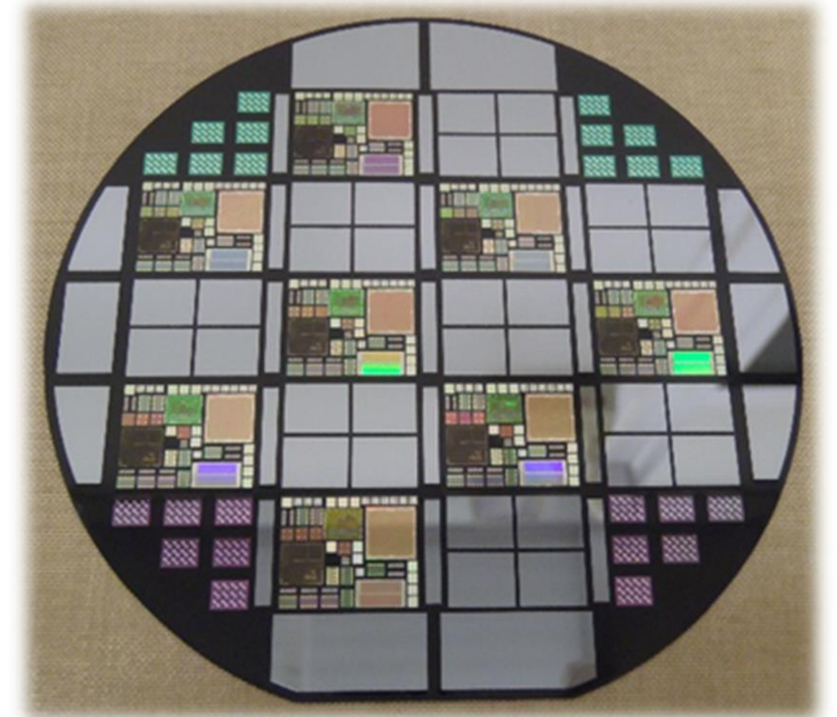
# i3 Microsystems Overview



- HSIP Benefits
  - Able to be brought out to BGA or SMT interfaces on both sides
  - Stacks as a subsystem – up to three slices
  - Scalable to larger wafer formats for volume production demand
  - Can incorporate extracted/recovered die for faster prototyping or lower volume orders



*HSIP Project Wafer, ready for our FO-WLP processing (note depopulated modules)*

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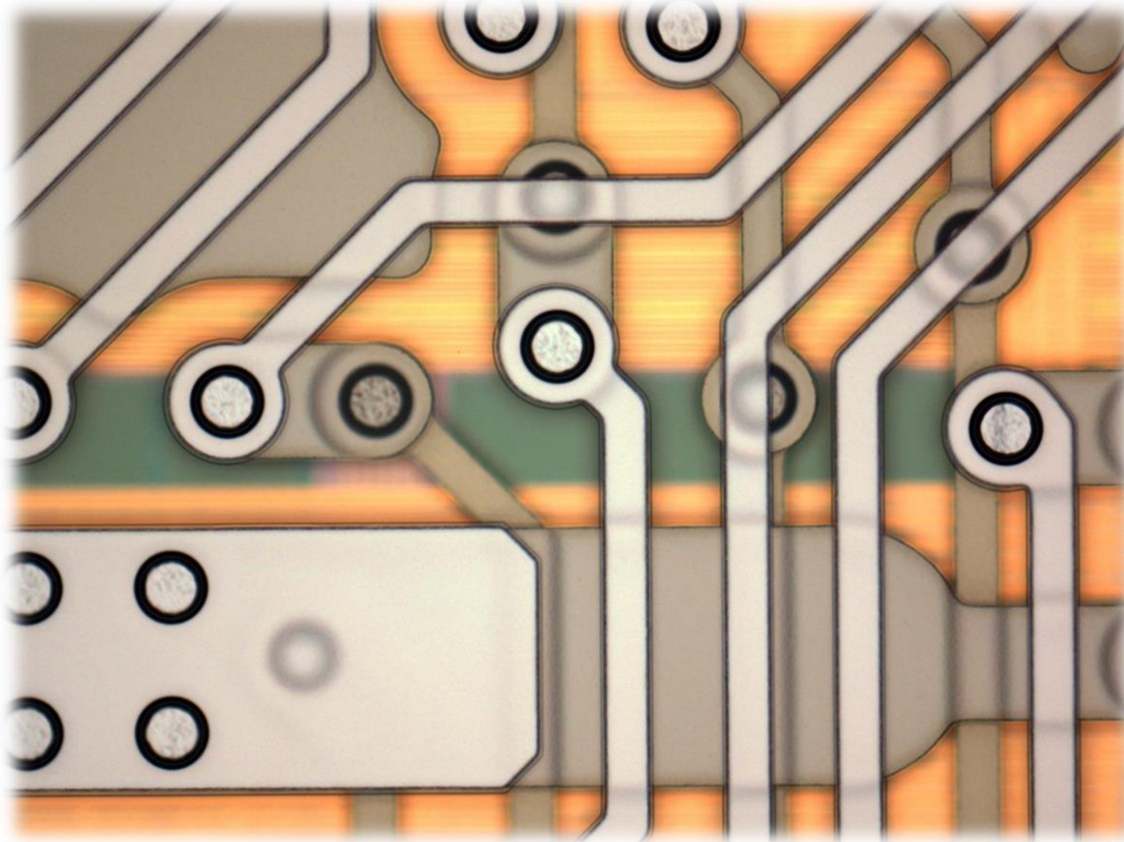
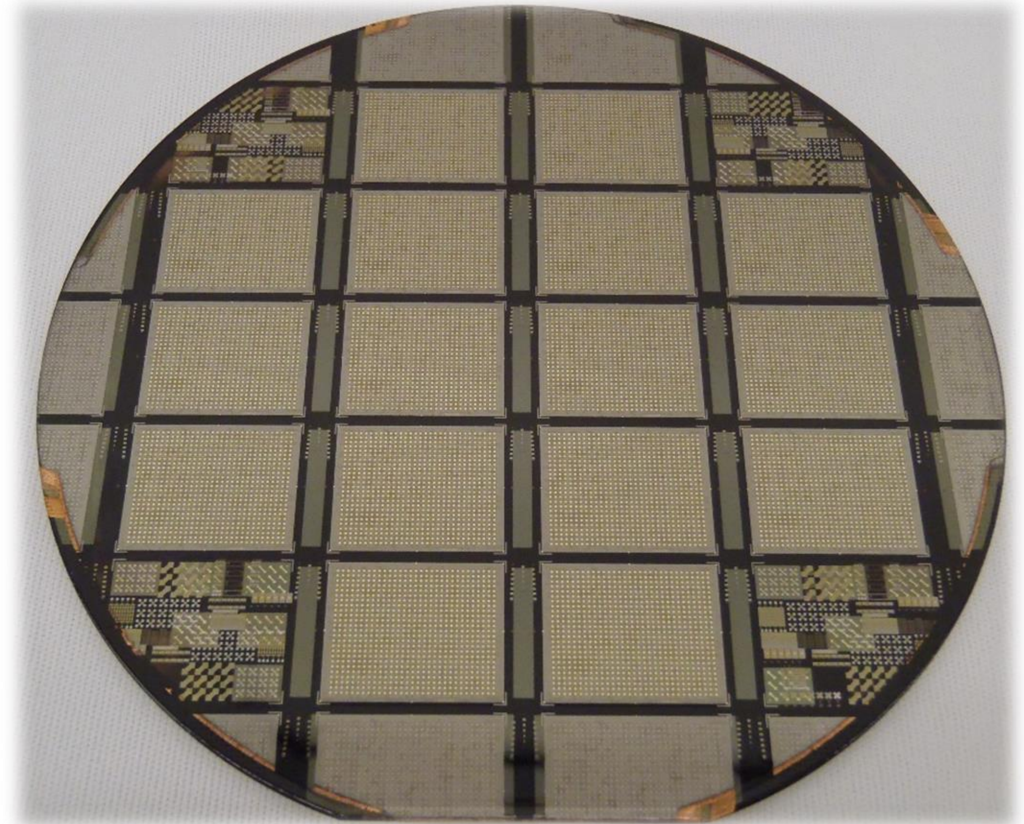
# i3 Microsystems Overview





*Example of HSIP interconnect routing layers with nominal 18-micron lines, 25-micron via. The image is showing three routing layers.*



*Typical completed HSIP wafer after 12 metal layers. 7 layers frontside, 5 layers backside.*

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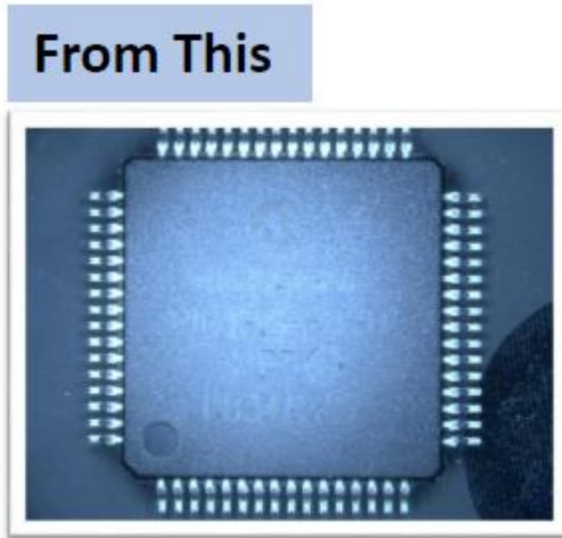
# i3 Microsystems Overview

- Die Harvesting – Die Extraction & Recovery (DER) Services

From This



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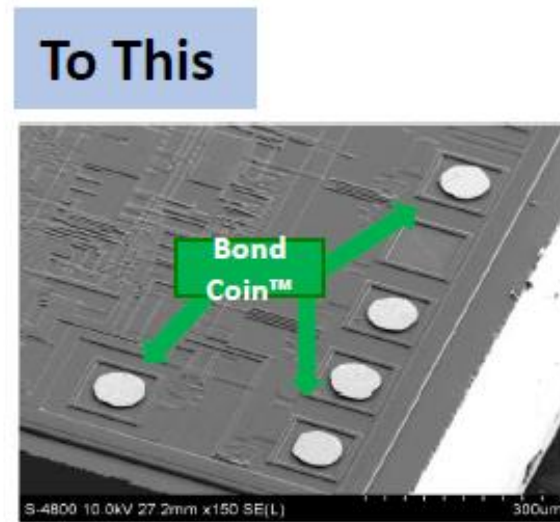
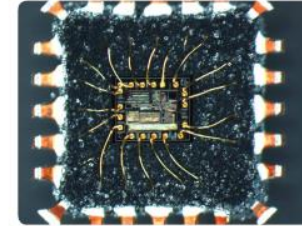
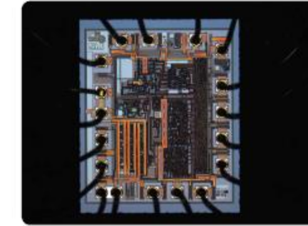


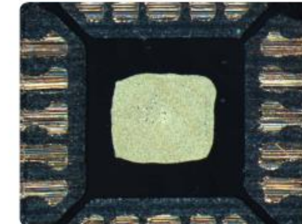

*DER is available as a Foundry Service*



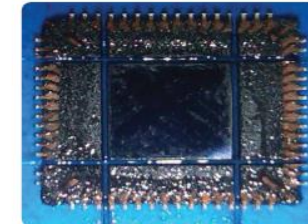


Initial Engineering Investigation / NRE

Back-Side Grind

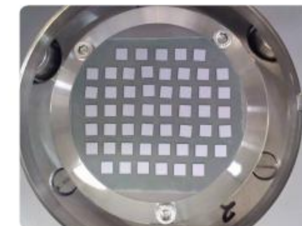


Die Pan Removal

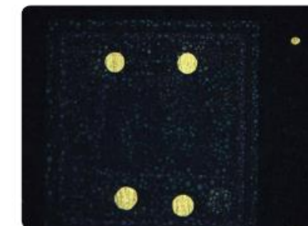


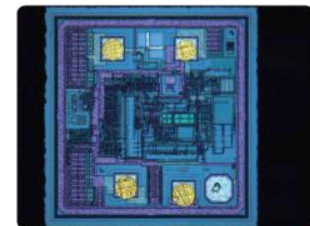
Dice to Precise Dimensions

Front-Side Grind & Diamond Lap



Back-Side Die Thinning





De-Encapsulation Etch Process

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# i3 Microsystems Overview



- HSIP Reliability Baseline

| Test | Result |
|---|---|
| E-Test - Temperature Acceptance Test (ATP) | PASS |
| Temperature Shock – MIL-STD-810G, Method 503.5, Procedure I-Steady State | PASS |
| Electrostatic Discharge – EN 61000-4-2, Level 4 | PASS |
| Electromagnetic Compatibility – MIL-STD-461F,RE101,RE102 & Radiated Susceptibility | PASS |
| Mechanical Shock – JEDEC Standard JESD22-B110A | PASS |
| Random Vibration – MIL-STD-810G, Method 514.5; system operating during exposure | PASS |
| High Temperature – MIL-STD-810G, Method 501.5; 2 day steady state +71°C | PASS |
| Low Temperature – MIL-STD-810G, Method 502.5; 2 day steady state -35°C | PASS |
| Low Pressure (Altitude) – MIL-STD-810G; system operating during exposure | PASS |
| Humidity – MIL-STD-810G, Method 507.5' system operating through test | PASS |
| Rain – MIL-STD-810G, Method 506.5, device in system format | PASS |
| 1000 hours of HTOL at 125 degrees C | PASS |
| 1000 hours of THB at 85%, 85C | PASS |
| 2000 thermal cycles -29C to +85C | PASS |

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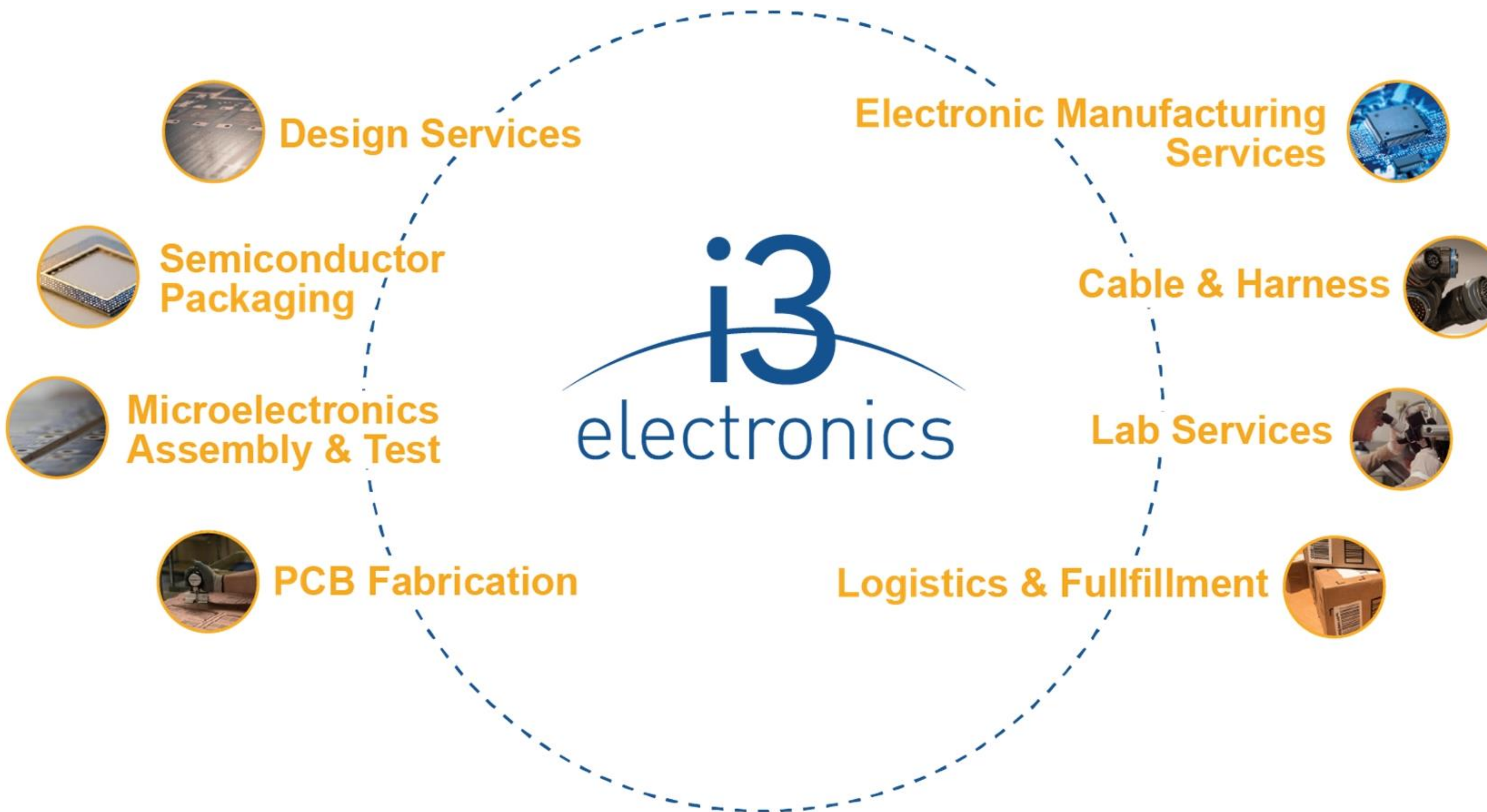
# i3 Electronics Overview

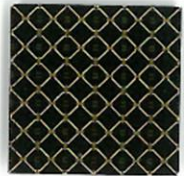


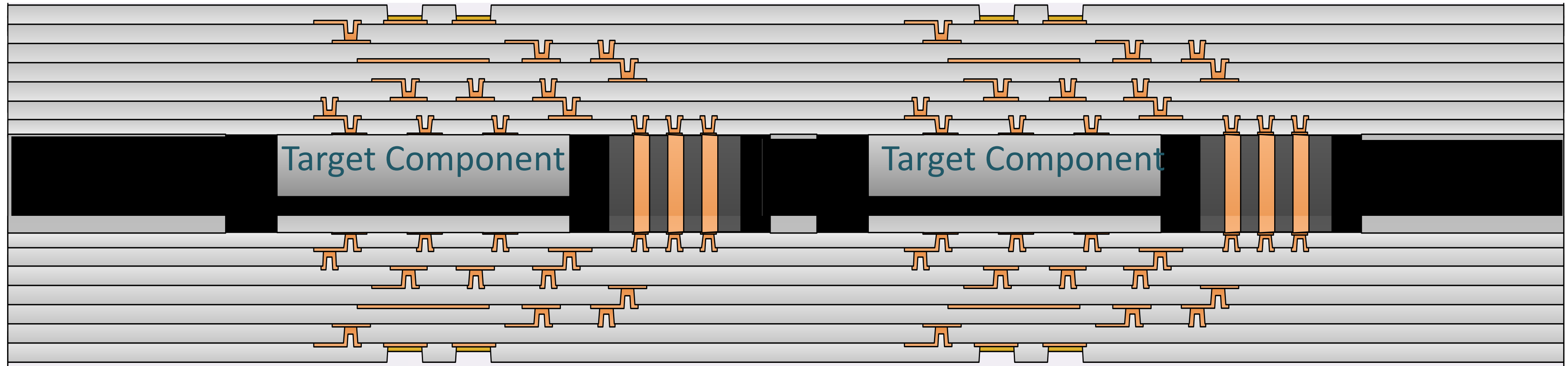


# HSIP Fabrication



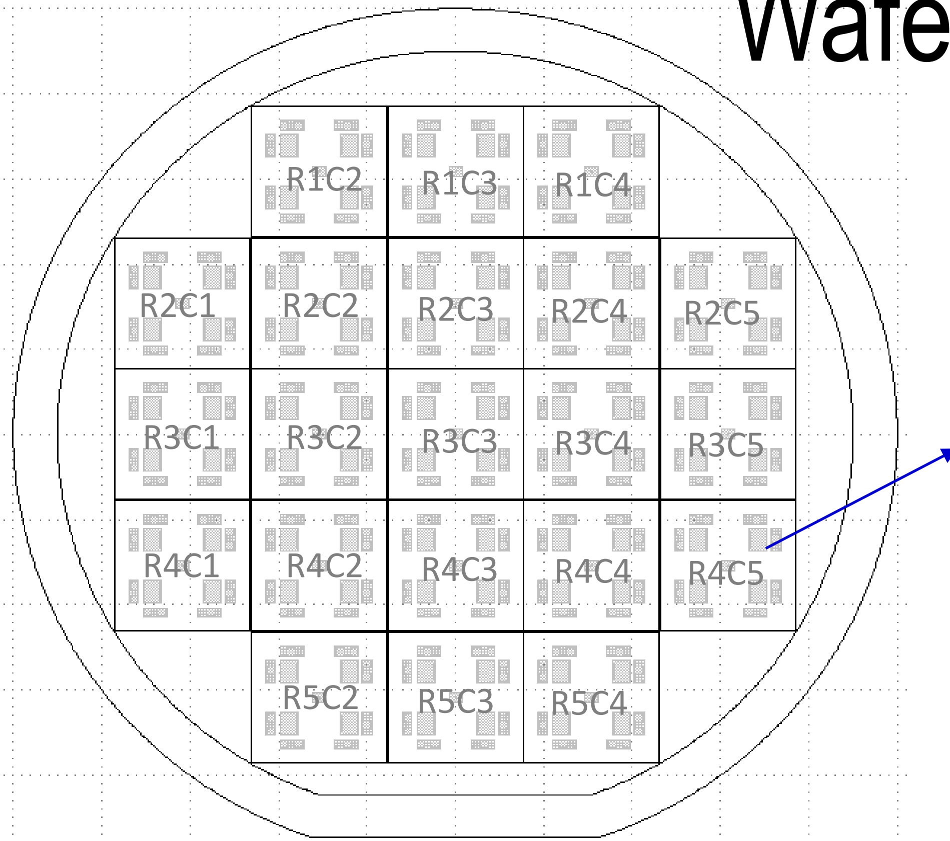
- HSIP Fabrication Discussion



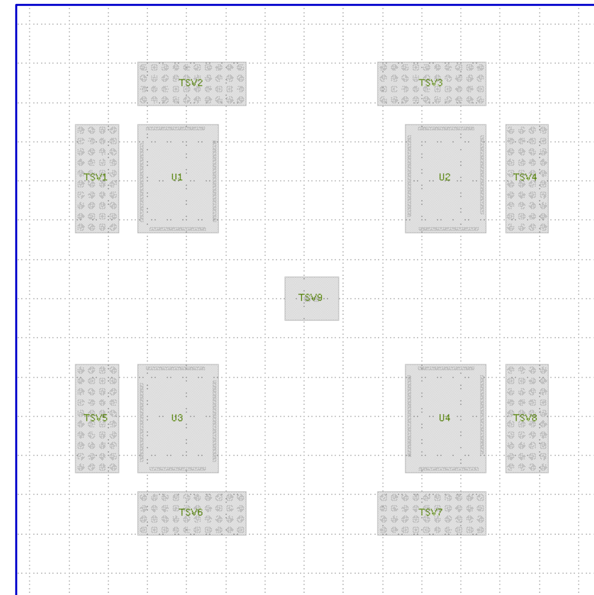



*Detail view of HSIP module Layers*

## Wafer Layout Detail




100MM wafer with 21 Module positions



15.4 x 15.4 mm exposure field per module
13 embedded die per module (4 active)

| Metal Layer | Percentage Metal of Module Area |
|---|---|
| MCM_F_MET1 | 5.8% |
| MCM_F_MET2 | 4.4% |
| MCM_F_MET3 | 0.6% |
| MCM_F_MET4 | 7.4% |
| MCM_B_MET1 | 3.1% |
| MCM_B_MET2 | 3.0% |
| MCM_B_MET3 | 2.2% |
| MCM_B_MET4 | 4.8% |
| MCM_F_SM | 2.2% |
| MCM_B_SM | 3.1% |

4 metal layers per side (low density patterns)

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# HSIP Fabrication

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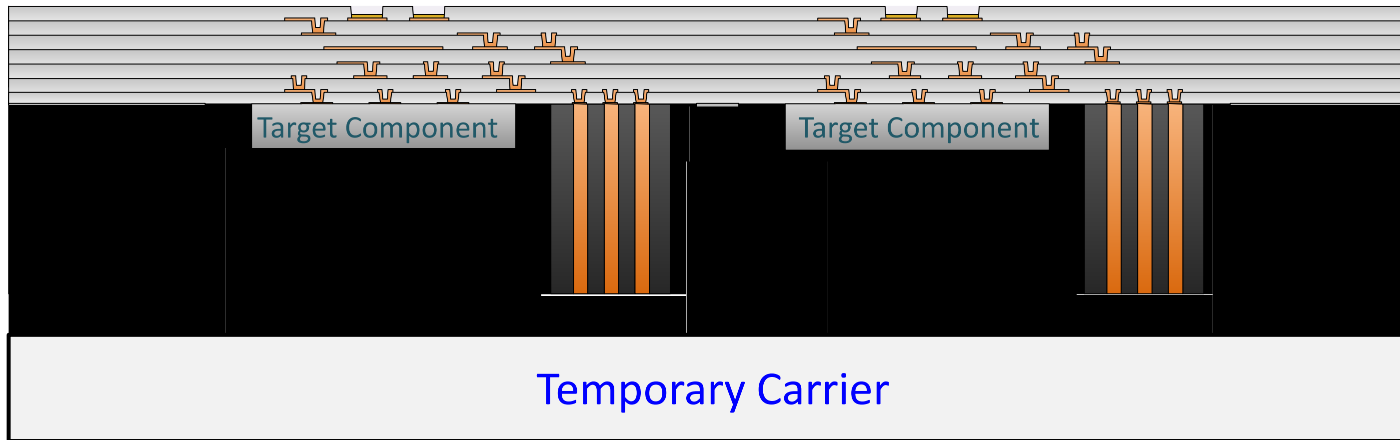
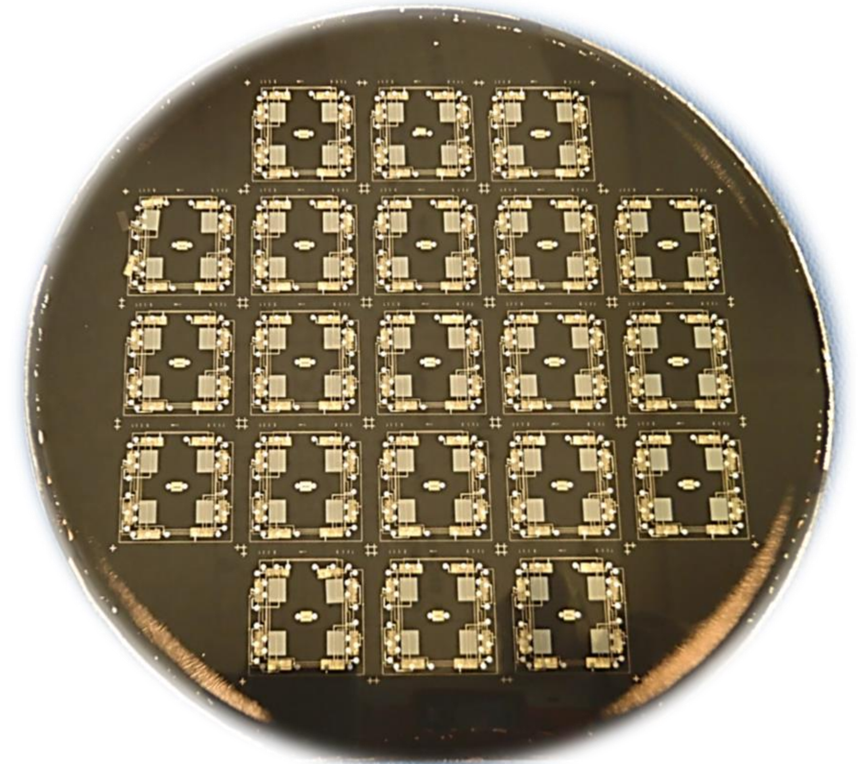
INSPIRED WORK



Molded (Reconstituted) wafer over carrier


actual wafer

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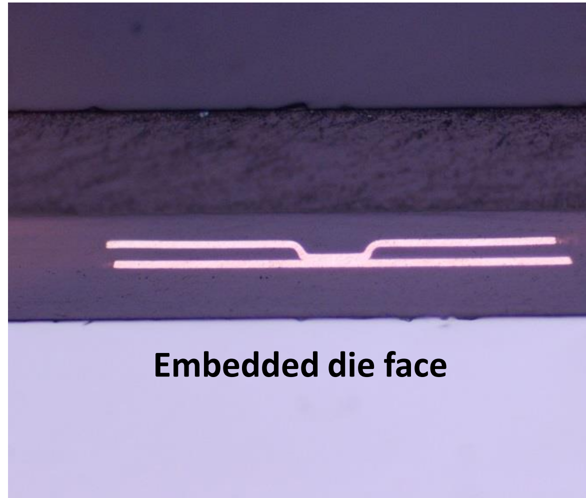
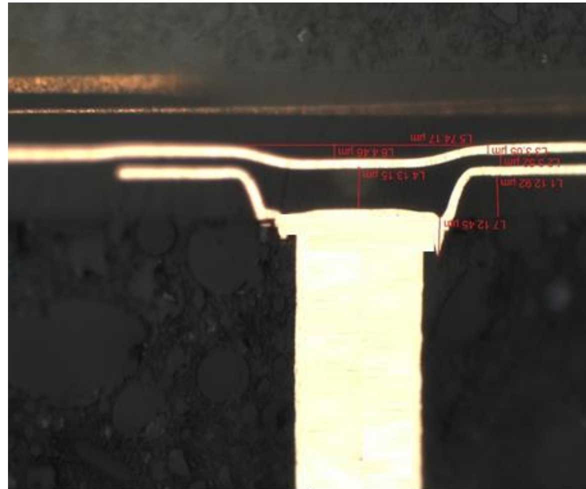
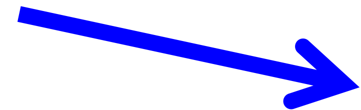
# HSIP Fabrication

BAE SYSTEMS
INSPIRED WORK





2-micron copper

5-micron dielectric

2-micron copper

15-micron dielectric (3 Layers)

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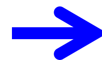
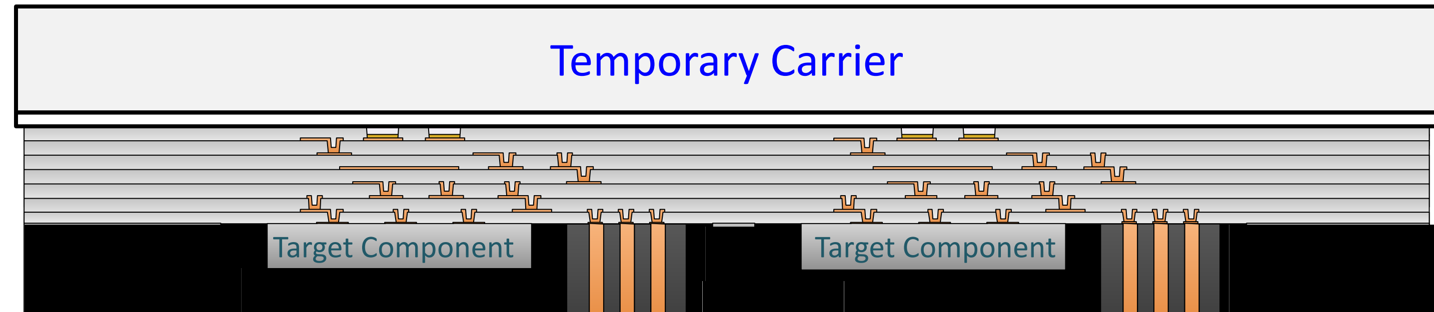
# HSIP Fabrication

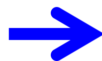
BAE SYSTEMS INSPIRED WORK

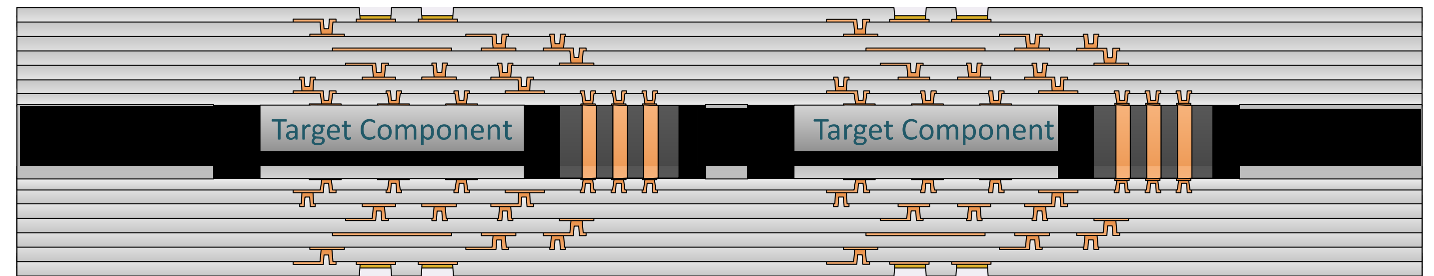
Backside Wafer Thinning
- Opens the Thru-Via contacts
- Brings core of device to target value






Completion of Backside Layers
- Temporary Carrier removed
- Device is singulated in normal dicing fashion



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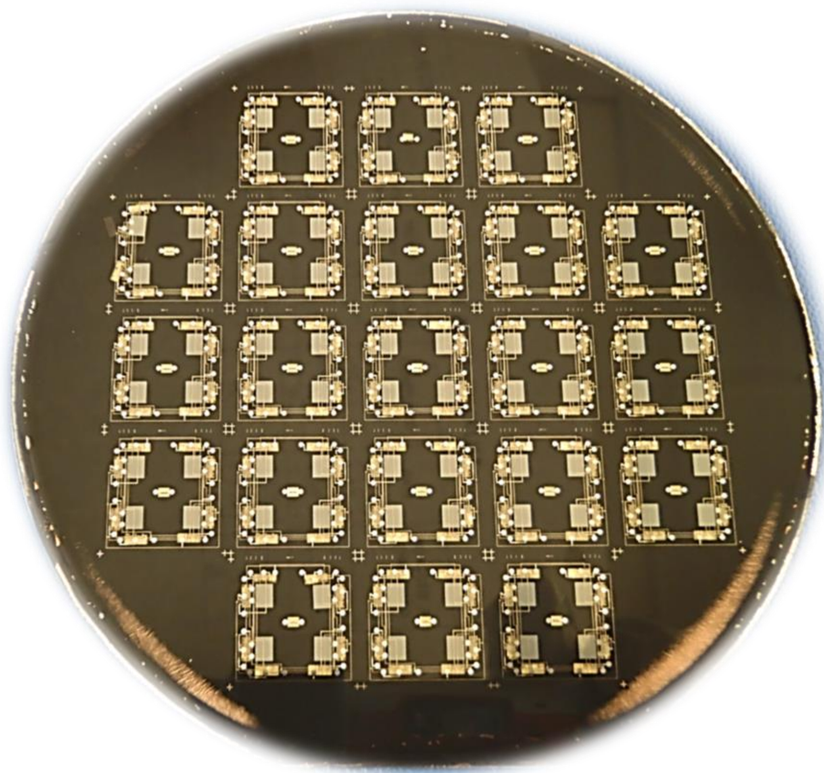
# HSIP Fabrication Results



- Discussion of the actual ACT TA2 – HSIP Build Results

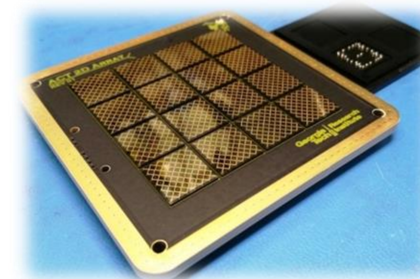


Georgia Tech

BAE
MMIC Fab

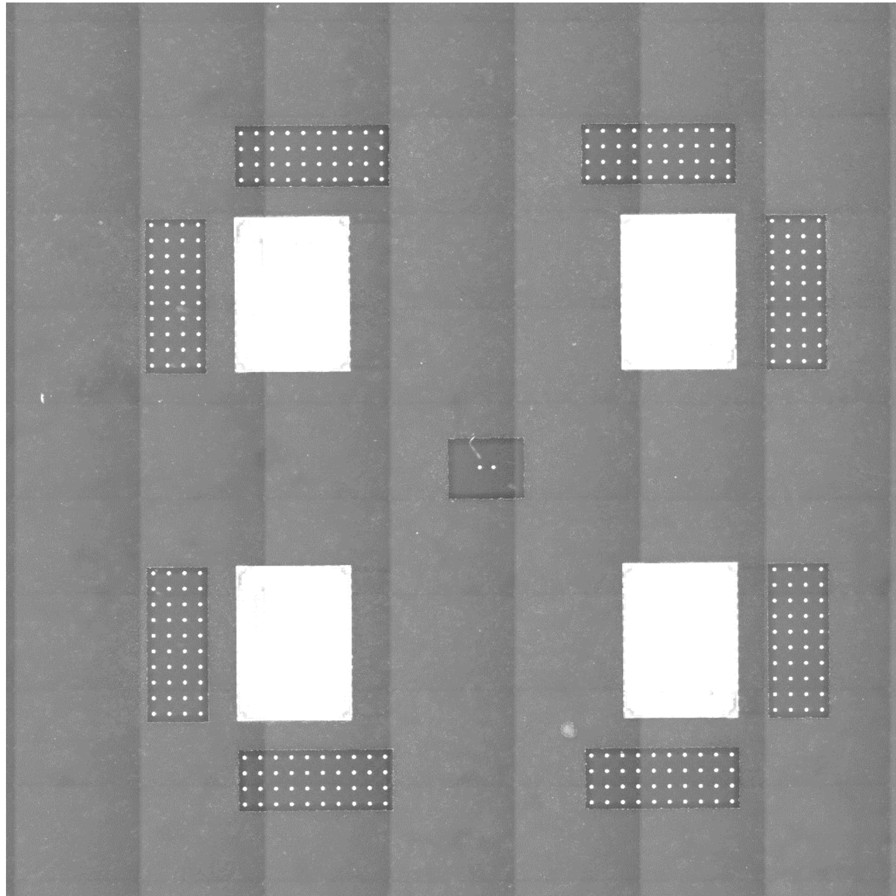
i3 Microsystems
HSIP Fab

i3 Electronics
Assembly Fab



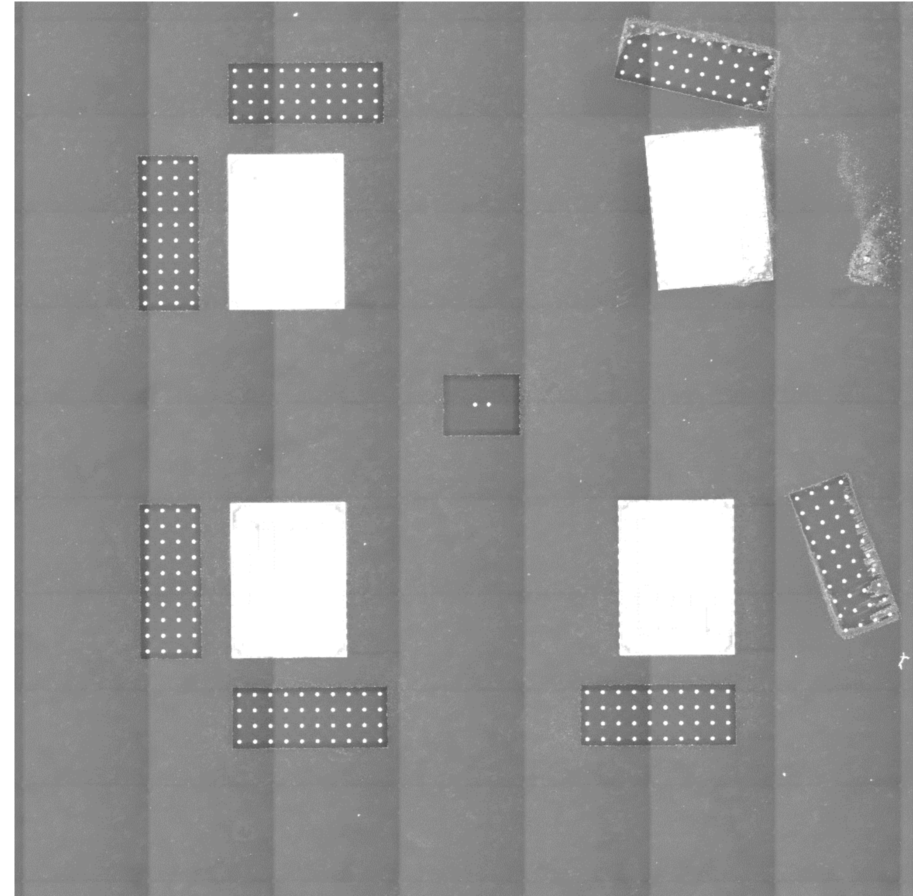
# HSIP Fabrication Results





GOOD RESULT

Die Shift from Wafer Molding



NOT AS GOOD

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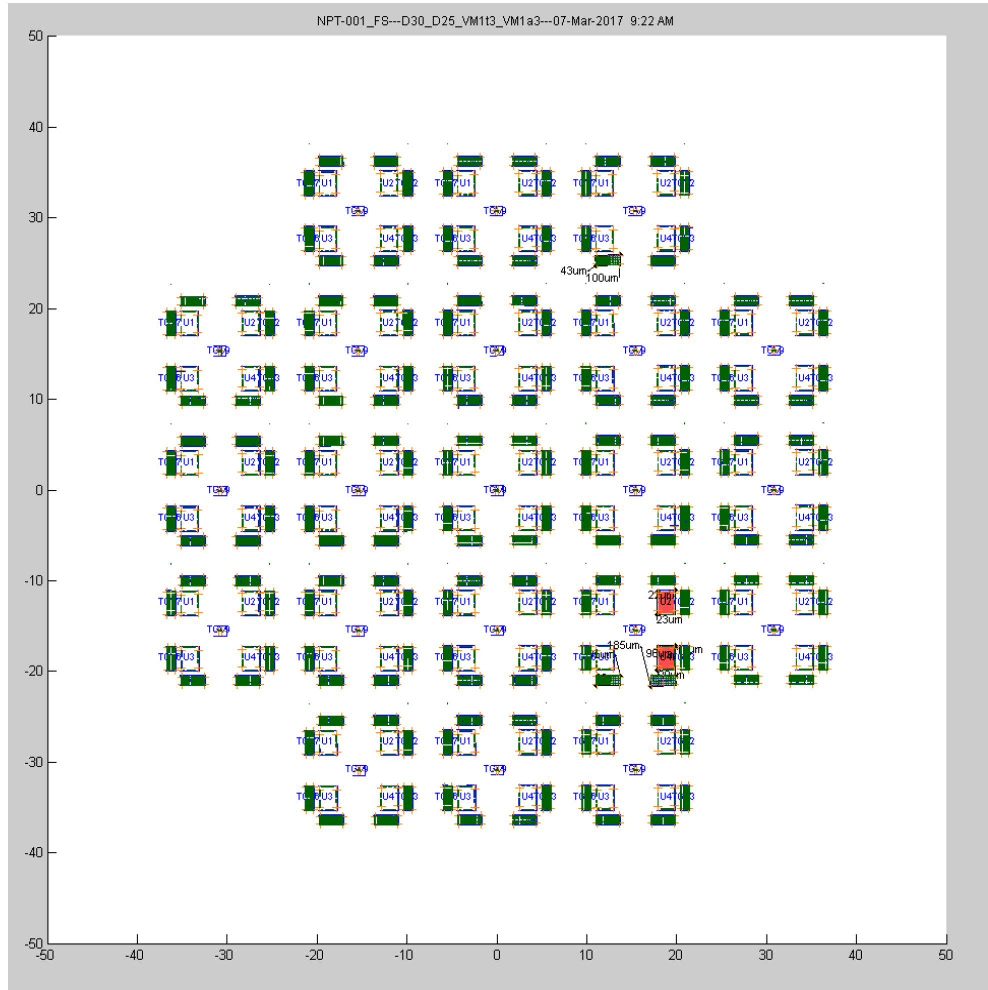
# HSIP Fabrication Results




| Fail Count | | | | |
|---|---|---|---|---|
| | R1C2 | R1C3 | R1C4 | |
| | 0 | 0 | 1 | |
| R2C1 | R2C2 | R2C3 | R2C4 | R2C5 |
| 0 | 0 | 0 | 0 | 0 |
| R3C1 | R3C2 | R3C3 | R3C4 | R3C5 |
| 0 | 0 | 0 | 0 | 0 |
| R4C1 | R4C2 | R4C3 | R4C4 | R4C5 |
| 0 | 0 | 0 | 4 | 0 |
| | R5C2 | R5C3 | R5C4 | |
| | 0 | 0 | 0 | |

10% Starting Yield Problem

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# HSIP Fabrication Results

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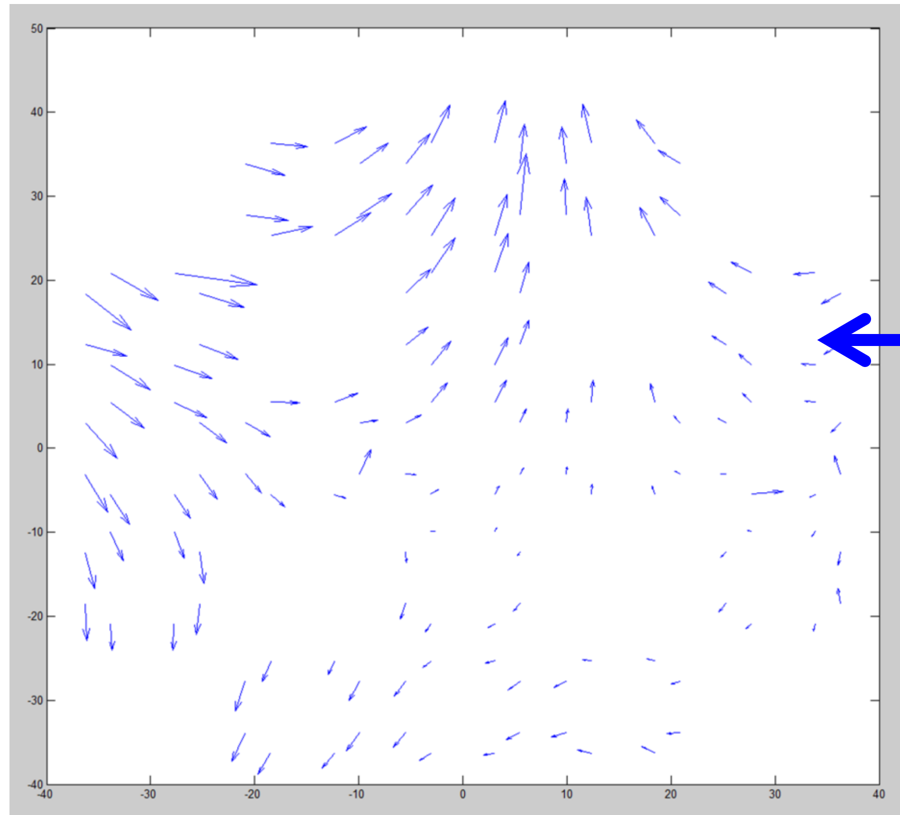
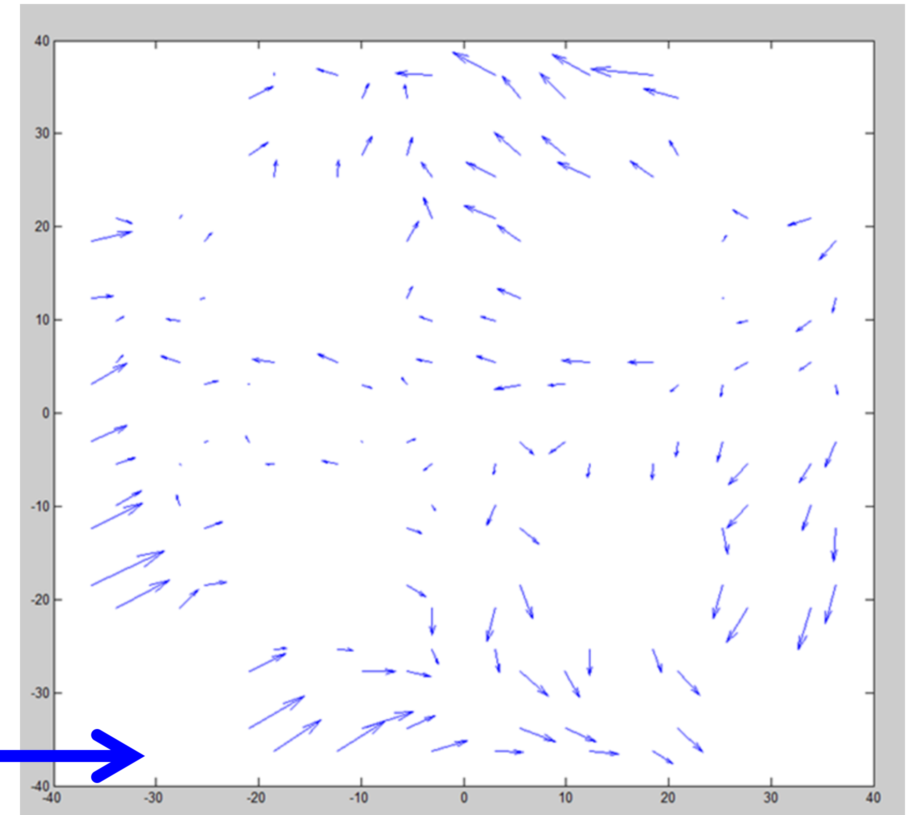
INSPIRED WORK




BEFORE ADJUSTMENTS

| Wafer Level Die Shift | |
|---|---|
| AVG | 48.7 |
| STD | 28 |
| MAX | 146.3 |
| MIN | 6.8 |

| Wafer Level Die Shift | |
|---|---|
| AVG | 9.2 |
| STD | 5.3 |
| MAX | 29.8 |
| MIN | 0.4 |




AFTER ADJUSTMENTS

Recipe-controlled wafer molding process allows for optimization relative to placed die area and density

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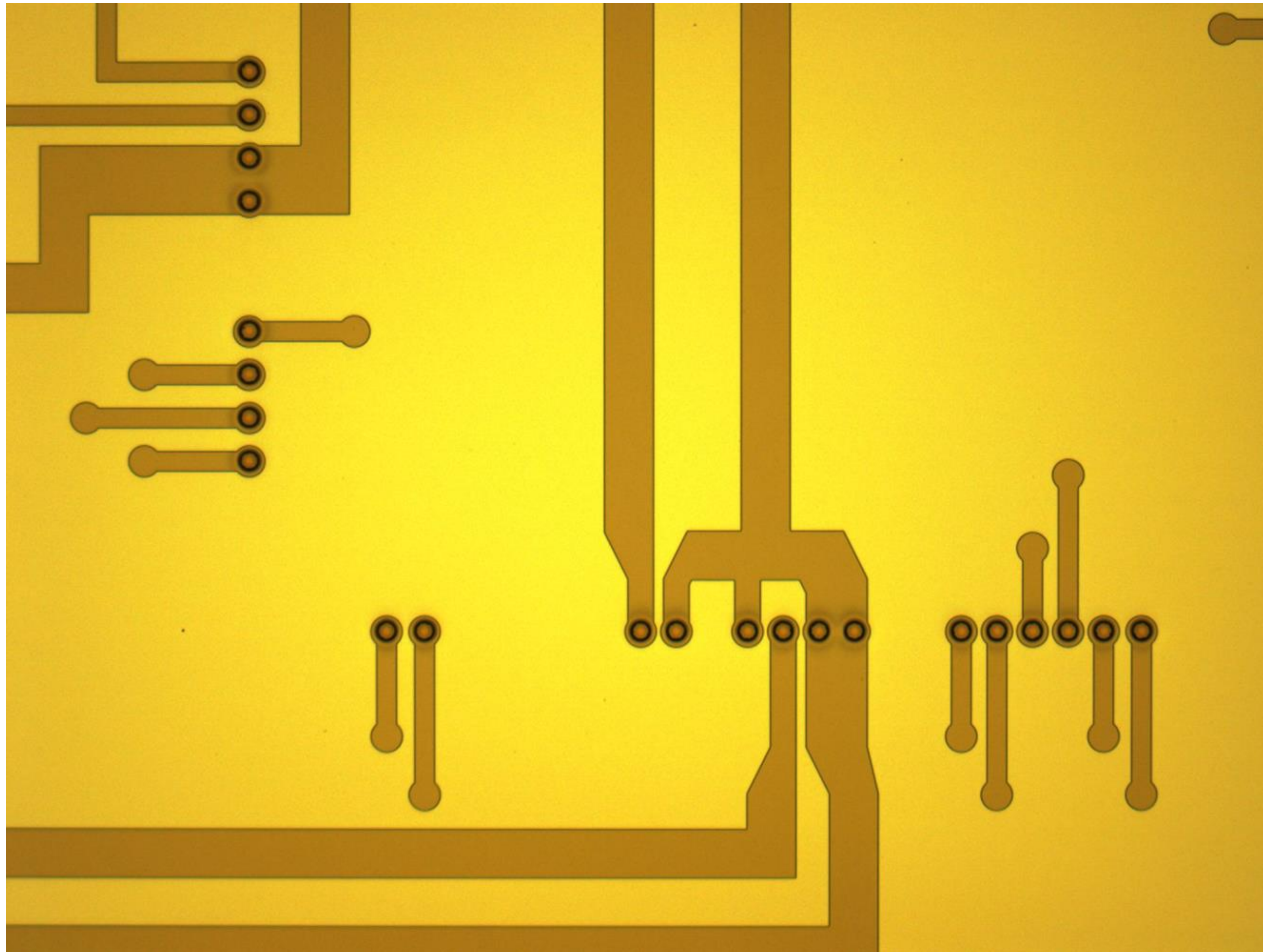
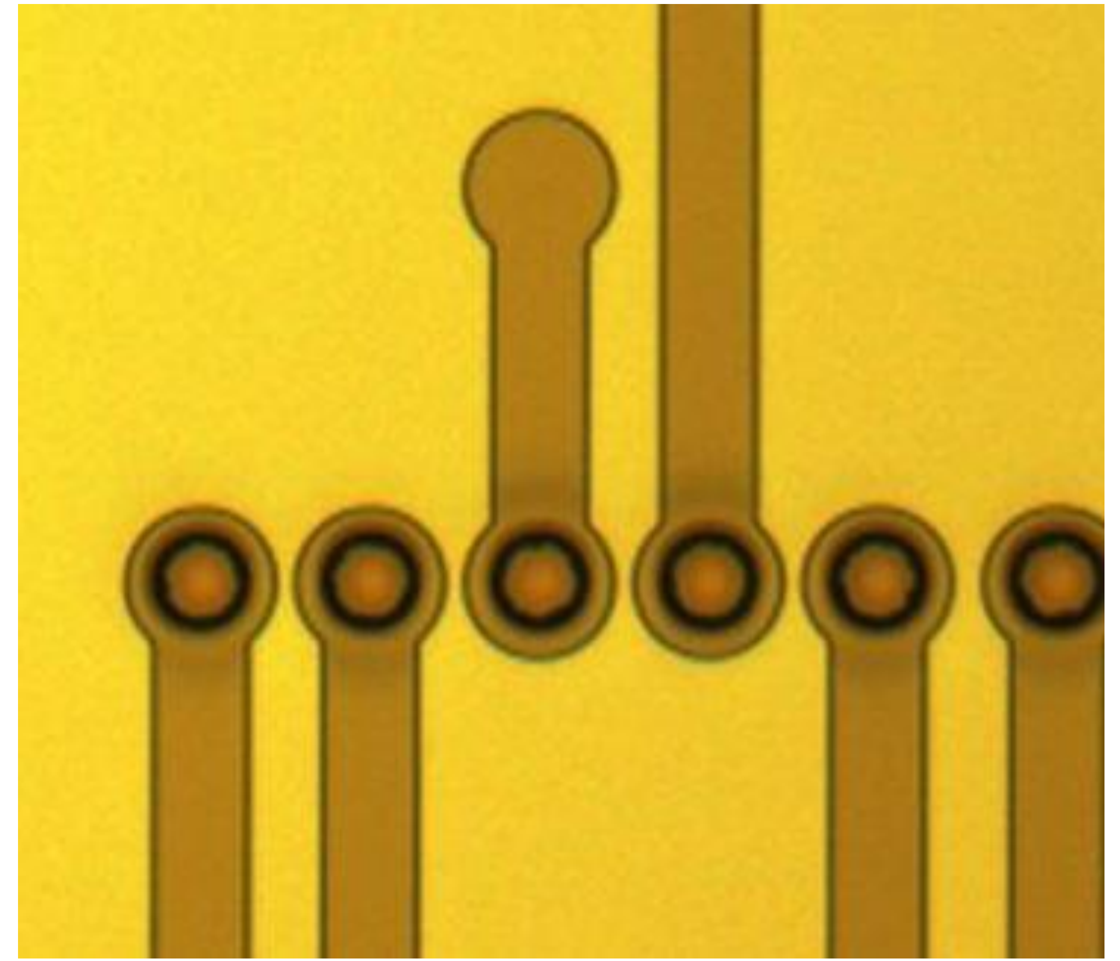
# HSIP Fabrication Results







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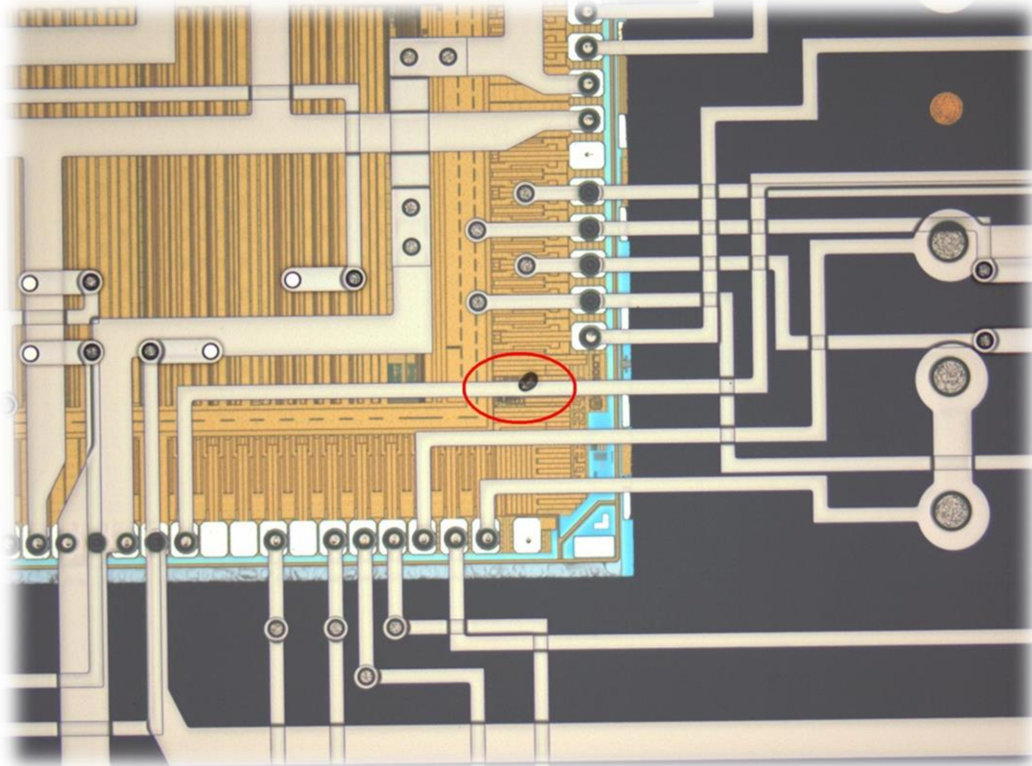
# HSIP Fabrication Results

BAE SYSTEMS
INSPIRED WORK



| Wafer ID | Good | Eng | Scrap | Wafer Yield |
|---|---|---|---|---|
| 001 | 12 | 5 | 4 | 57% |
| 002 | 17 | 1 | 3 | 81% |
| 003 | 17 | 2 | 2 | 81% |
| 004 | 17 | 1 | 3 | 81% |
| Bin Yields | 75% | 11% | 14% | |

Across all 4 wafers and 32 metal layers, the yield was **75%** for all visual non-conformances, including die shift

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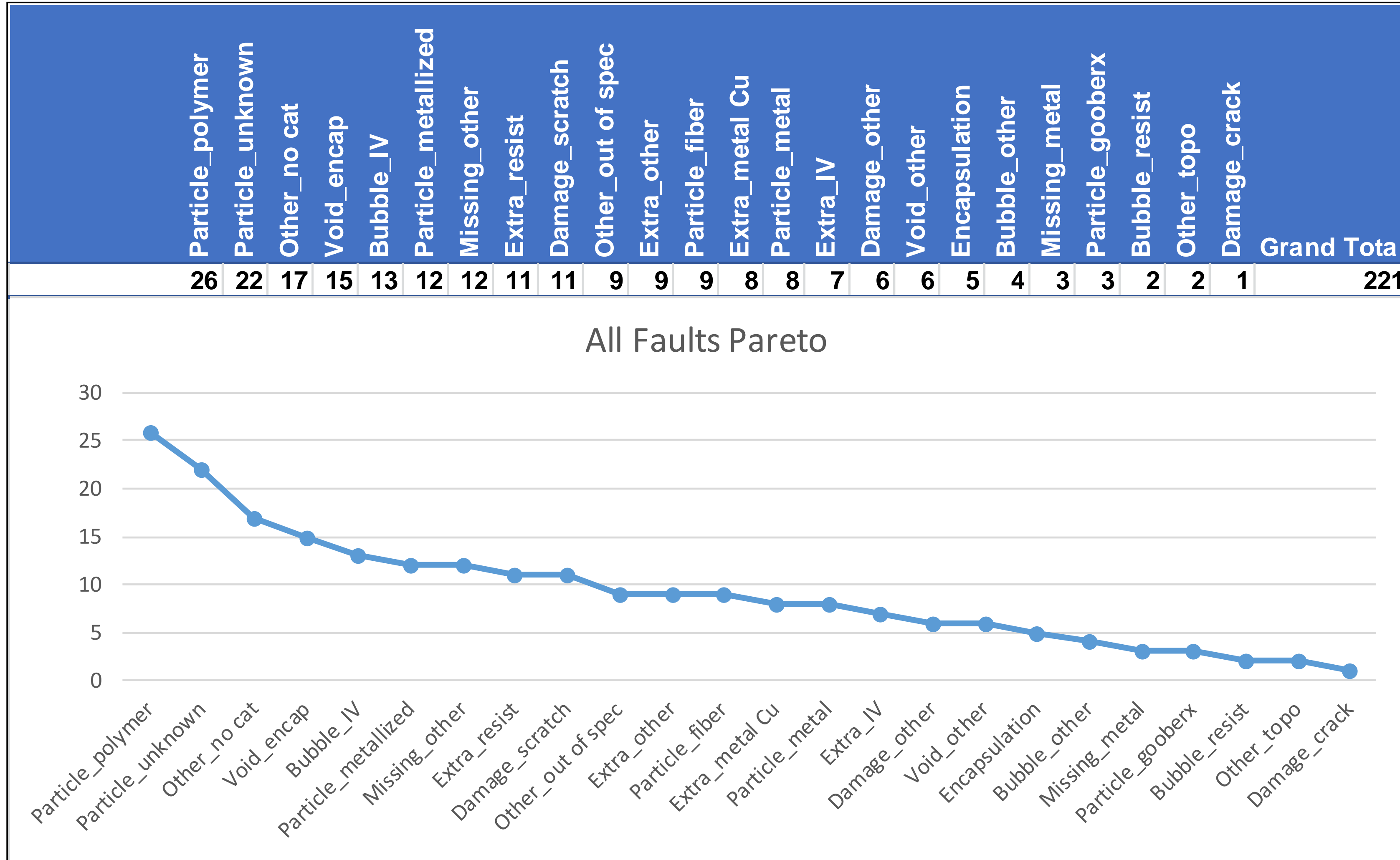
# HSIP Fabrication Results



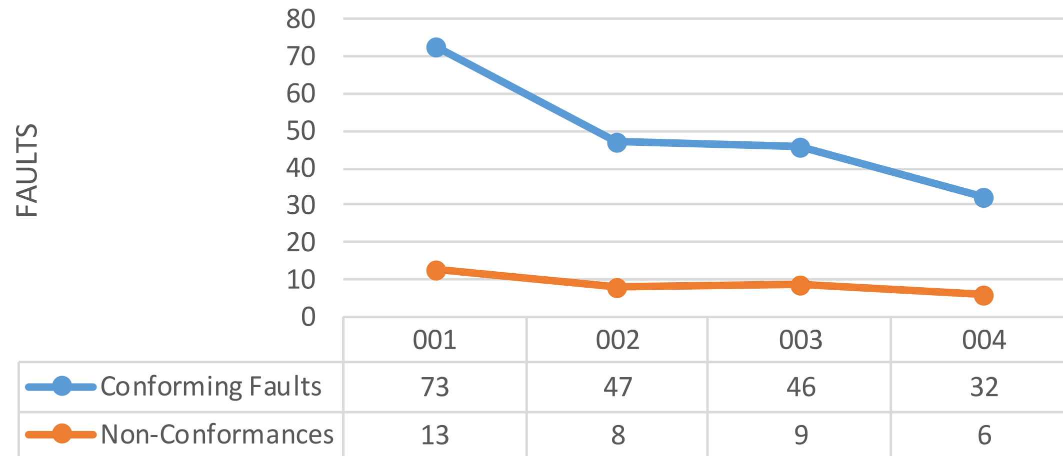
| Particle_polymer | Particle_unknown | Other_no cat | Void_encap | Bubble_IV | Particle_metallized | Missing_other | Extra_resist | Damage_scratch | Other_out of spec | Extra_other | Particle_fiber | Extra_metal Cu | Particle_metal | Extra_IV | Damage_other | Void_other | Encapsulation | Bubble_other | Missing_metal | Particle_gooberx | Bubble_resist | Other_topo | Damage_crack | Grand Total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 26 | 22 | 17 | 15 | 13 | 12 | 12 | 11 | 11 | 9 | 9 | 9 | 8 | 8 | 7 | 6 | 6 | 5 | 4 | 3 | 3 | 2 | 2 | 1 | 221 |

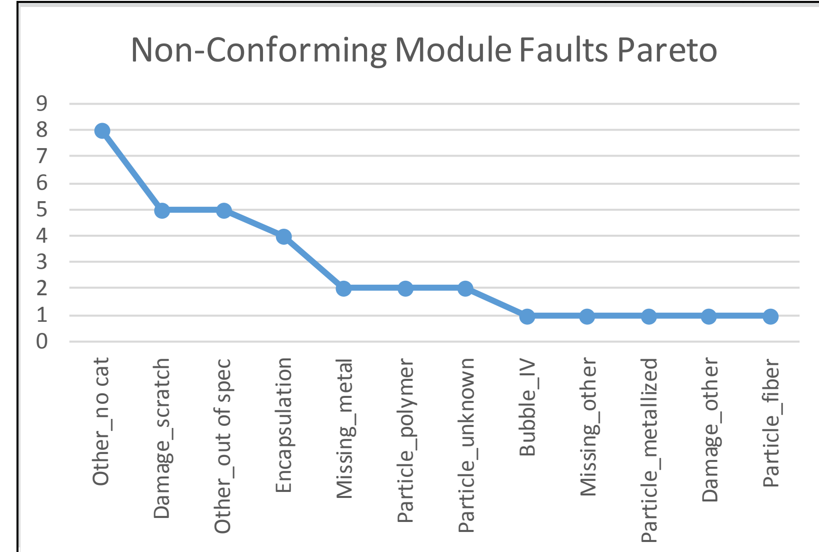


I3 MICROSYSTEMS INC PROPRIETARY INFORMATION

# HSIP Fabrication Results

| Count of Status | Status2 / Status: Conforming Faults | Non-Conformances | Grand Total |
|---|---|---|---|
| Wafer | | | |
| 001 | 73 | 13 | 86 |
| 002 | 47 | 8 | 55 |
| 003 | 46 | 9 | 55 |
| 004 | 32 | 6 | 38 |
| **Grand Total** | **198** | **36** | **234** |

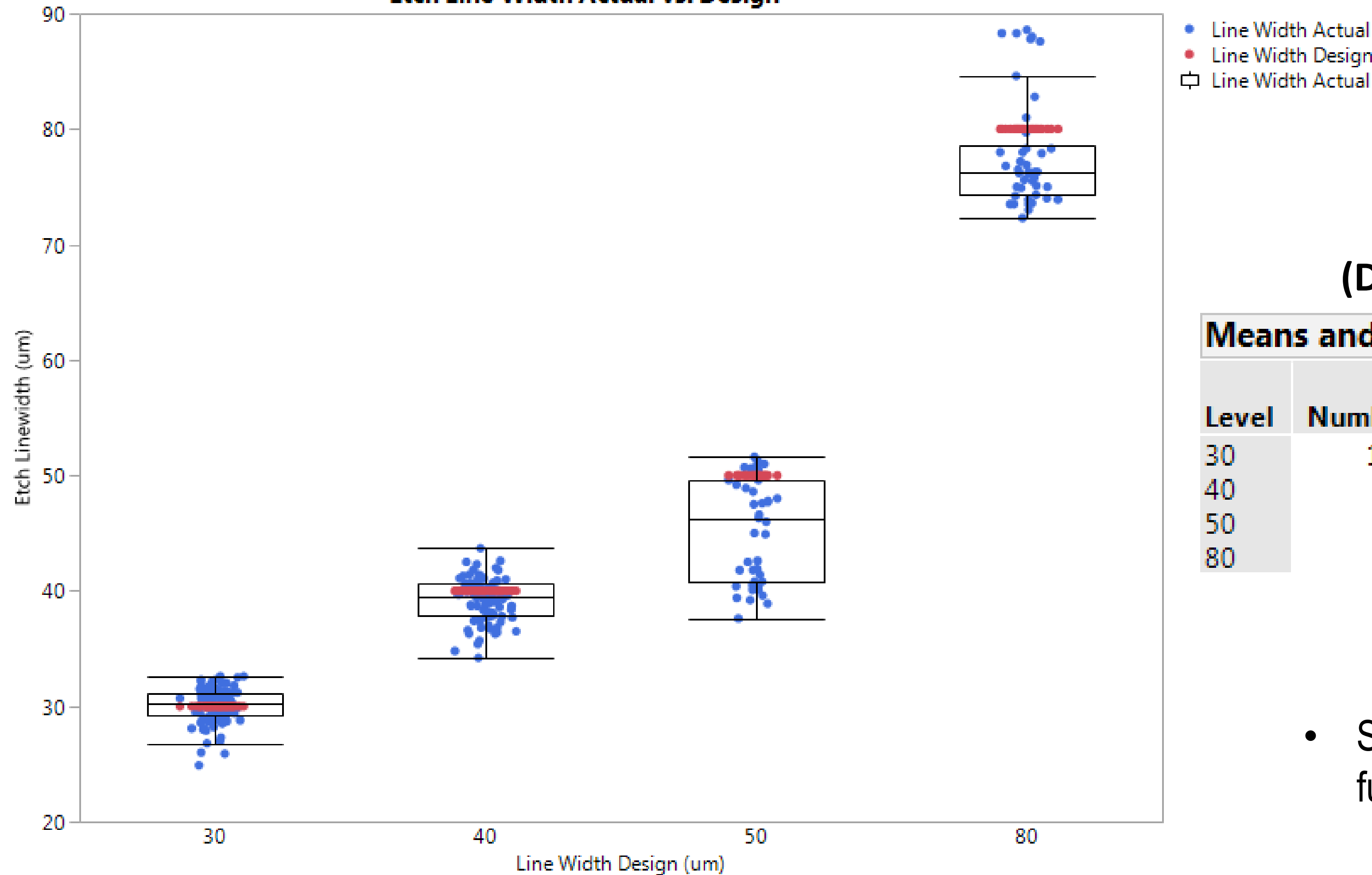



| Non-Conforming Faults / Subcategory | Other_no cat | Damage_scratch | Other_out of spec | Encapsulation | Missing_metal | Particle_polymer | Particle_unknown | Bubble_IV | Missing_other | Particle_metallized | Damage_other | Particle_fiber | Gra |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| die | 4 | 2 | 3 | 2 | | 1 | 1 | | | | | | 13 |
| pad | 1 | 1 | | | 1 | | 1 | | | | | | 4 |
| space_active | | | | 2 | | | | 1 | | 1 | | | 4 |
| space_inactive | | | | | | | | | 1 | | | | 1 |
| trace_in | | 2 | | | 1 | | | | | | | | 3 |
| via | 3 | | 2 | | | 1 | | | | | 1 | 1 | 8 |
| **Grand Total** | **8** | **5** | **5** | **4** | **2** | **2** | **2** | **1** | **1** | **1** | **1** | **1** | **33** |

# HSIP Fabrication Results






**Etched Line Width Reduction**
**(Delta to Design, all data in microns)**

**Means and Std Deviations**

| Level | Number | Mean | Std Dev | Std Err Mean | Lower 95% | Upper 95% |
|---|---|---|---|---|---|---|
| 30 | 105 | 0.0943 | 1.50076 | 0.14646 | -0.196 | 0.385 |
| 40 | 84 | -0.7762 | 1.90583 | 0.20794 | -1.190 | -0.363 |
| 50 | 42 | -4.7500 | 4.47695 | 0.69081 | -6.145 | -3.355 |
| 80 | 42 | -2.0857 | 4.88999 | 0.75454 | -3.610 | -0.562 |

- Some etch process tuning remains for future wafer builds of this design

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# HSIP Fabrication Results

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| Date | Wafer | Module | Module Thickness Core (um) | Module Thickness Total (um) | Wafer Bond Thickness (um) | Module Bow (um) | XY Size (um) |
|---|---|---|---|---|---|---|---|
| 6/13/2017 | NPT-001 | | | | | 9.7 | |
| 6/13/2017 | NPT-001 | | | | | 14.4 | |
| 6/13/2017 | NPT-001 | | | | | 15.6 | |
| 6/13/2017 | NPT-001 | | | | | | |
| 6/13/2017 | NPT-001 | | | | | | |
| 6/13/2017 | NPT-002 | R5C2 | 263.4 | 338.1 | 42.2 | 15.9 | 14606.4 |
| 6/13/2017 | NPT-002 | R4C4 | 266.0 | 333.3 | 45.4 | 17.8 | 14597.2 |
| 6/13/2017 | NPT-002 | R1C2 | 268.7 | 333.9 | 46.5 | 7.4 | 14604.3 |
| 6/13/2017 | NPT-002 | R2C3 | 268.2 | 338.1 | 45.9 | 1.6 | 14601.3 |
| 6/13/2017 | NPT-002 | R3C5 | 263.4 | 335.8 | 46.5 | 18.3 | 14591.7 |
| 7/24/2017 | NPT-003 | R1C3 | 270.7 | 345.9 | 41.3 | 12.6 | 14625.6 |
| 7/24/2017 | NPT-003 | R1C4 | 268.5 | 344.8 | 43.4 | 16.3 | 14608.6 |
| 7/24/2017 | NPT-003 | R3C1 | 272.8 | 346.4 | 38.7 | 19.7 | 14621.6 |
| 7/24/2017 | NPT-003 | R4C2 | 269.6 | 344.8 | 45.6 | 20.0 | 14593.8 |
| 7/24/2017 | NPT-003 | R4C4 | 273.2 | 351.8 | 48.0 | 13.2 | 14598.8 |
| 6/13/2017 | NPT-004 | R2C1 | 273.8 | 350.5 | 41.3 | 24.9 | 14557.9 |
| 6/13/2017 | NPT-004 | R2C3 | 271.2 | 348.9 | 46.6 | 31.4 | 14568.0 |
| 6/13/2017 | NPT-004 | R3C2 | 271.7 | 352.6 | 56.3 | 30.4 | 14576.1 |
| 6/13/2017 | NPT-004 | R4C4 | 278.1 | 354.2 | 42.9 | 23.2 | 14575.0 |
| 6/13/2017 | NPT-004 | R5C3 | 277.6 | 353.7 | 38.0 | 1.0 | 14572.0 |

**Final Module Bow**
Mean 14.5um
Stdev 11.2um

**Final Module Thickness**
Mean 346.4um
Stdev 7.0um

**Final Module Core**
Mean 270.5um
Stdev 4.4um

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# HSIP Fabrication Results

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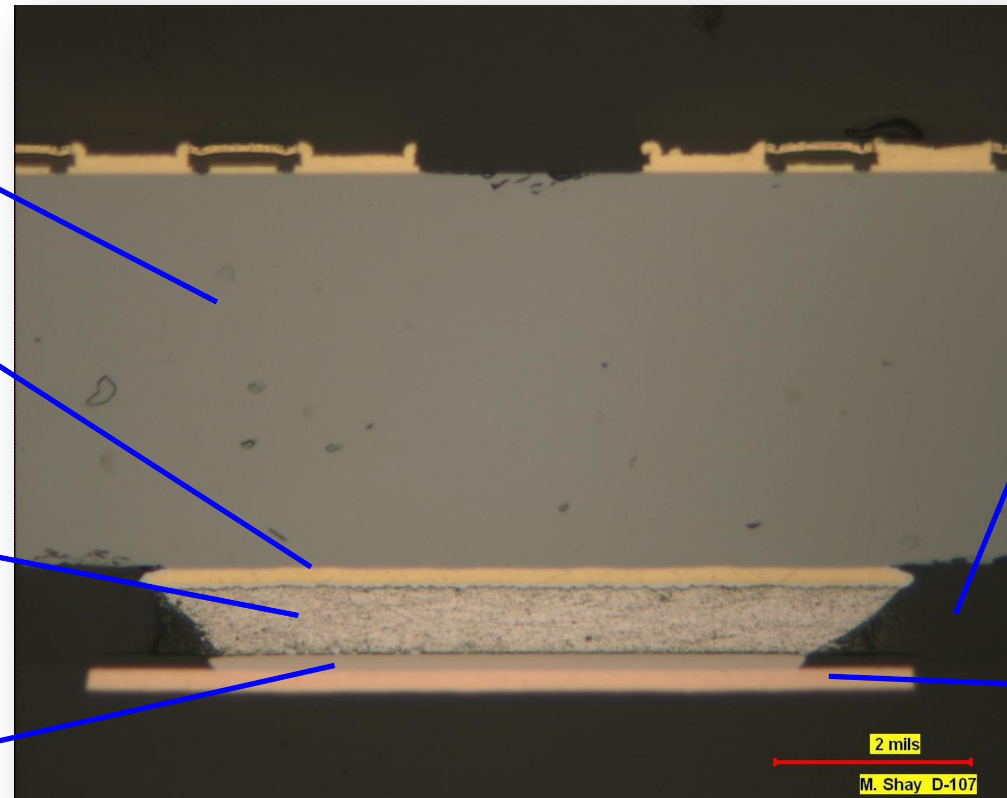
BAE MMIC die

BAE MMIC gold pads

i3 Electronics Solder

i3 Microsystems UBM




i3 Microsystems Solder Mask

i3 Microsystems copper pads

*Cross-section of assembled stack, courtesy of i3 Electronics, 2017*

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# Conclusion

BAE SYSTEMS
INSPIRED WORK

- HSIP technology can produce robust electronic components that meet next-generation packaging requirements for tightly packed integrations in order to achieve the lowest power, weight, and size while enabling new and exciting system concepts for designers

***THANK YOU***

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